Application note

STM32G4 ADC use tips and recommendations

Introduction

The STM32G4 Series microcontrollers are designed to support high-end analog applications. These MCUs embed high-performance analog peripherals (ADCs, DACs, COMPs, OPAMPs, reference voltage) and high-performance digital components such as their Arm® Cortex®-M4 CPU, mathematical accelerators, DMA and high-resolution timer among others.

This application note presents specific properties of the embedded ADC in the STM32G4 Series and an introduction on how properly design an application using those specific ADCs properties.

This document introduces the specific ADC properties that influence the ADC accuracy of a final application and explains how to correctly design applications hardware and software to improve the ADC accuracy for various application cases.

1 STM32G4 ADC features

This document uses as reference the specific STM32G4 ADC features listed in the table below. This table presents the basic numeric values used as reference in the following sections.

Table 1. ADC features on STM32G4 Series

Features	Values for STM32G4 Series
Number of ADCs	Up to 5
Number of input channels	Up to 42
ADC principle	Successive approximation register (SAR)
ADC clock frequency	Up to 60 MHz
Sampling rate	Up to 4 Msps
Sampling time	2.5 to 640.5 [ADC clock periods]
Supply voltage	V_{DDA} = 1.62 to 3.6 V
Reference voltage	On dedicated VREF+ pin(1) (internal or external), V_{REF+} = 1.62 v to V_{DDA} (see datasheet)
Triggers	From external pins or internal peripherals (timers)
Conversion modes	Single, continuous, scan-selected channels, discontinuous mode
Others	Offset calibration, analog watchdog, hardware oversampling, offset compensation, gain compensation, interleaved mode (two ADCs coupled), sampling time controlled by triggers edges, bulb mode sampling

1. *In the LQFP128-pin packages, two VREF+ pins are available.*

For more detailed information on ADC features and characteristics on STM32G4 Series, refer to the corresponding products datasheet and reference manual (RM0440) available at www.st.com.

The STM32G4 Series are Arm®-based devices.

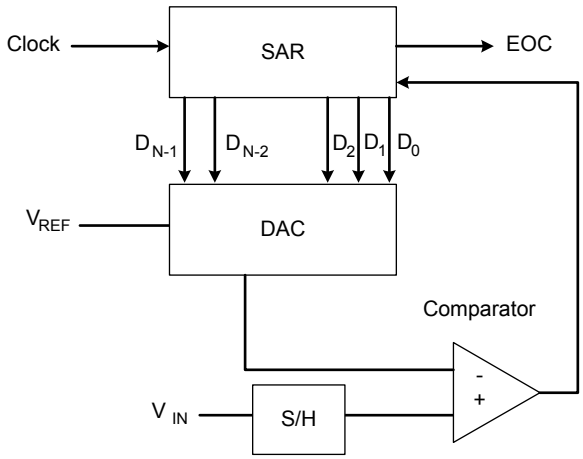
Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Maximum ADC speed

2.1 Successive approximation principle

The ADC in STM32G4 Series is based on the successive approximation register principle. This principle is depicted in the figure below:

Figure 1. ADC operation based on successive approximation principle



The input voltage (V_{IN}) is sampled by the sample-and-hold block (S/H) (as voltage on sampling capacitor) to have stable voltage during conversion time. This sampled voltage is then compared by the comparator with known voltage. This known voltage is provided by the DAC that is supplied by the reference voltage V_{REF}.

The DAC digital input is generated by the successive approximation register (SAR) as a digital word. This digital word is generated according to the result from the comparator and is based on the successive approximation principle. The SAR initially generates a word corresponding to a half voltage range. If the result from the comparator is zero (meaning that input voltage is less than ½ V_{REF}), then, in the second step, the word corresponding ¼ V_{REF} is generated by the SAR . In each approximation step, the SAR adds or subtracts 2^n weight according to the current step result from the comparator. After N steps, the SAR generates a final word that is the ADC digital result. The generated analog voltage is close to the measured voltage (with maximum ½ LSB difference).

2.2 Maximum ADC speed in successive approximation

The maximum ADC speed is given for the successive approximation principle by the DAC speed and the comparator speed (see Figure 1). In each successive approximation clock cycle, the DAC must set the correct stable analog voltage on its output (with ½ LSB accuracy) and the comparator must provide the result at the end of each cycle the final result.

For example: If ADC clock is 60 MHz, then each ADC clock cycle takes 1 / 60MHz = 16 ns. This 16 ns time represents the DAC output stabilization time plus the propagation delay of the comparator.

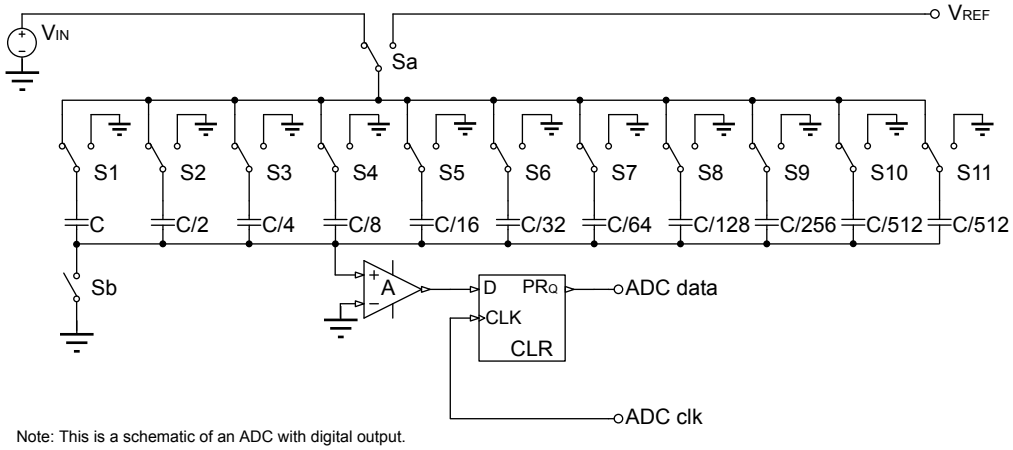
2.3 Switched capacitors

The ADC principle in STM32 MCUs is based on successive approximation where the DAC is based on switched capacitors network. The capacitors network implementation is technologically acceptable and precise. The advantage of this solution is that the capacitive network works also as sampling capacitor. So there is no need to have one more additional sampling capacitor.

The principle of this implementation is explained in section 1. *ADC internal principle* of the application note *How to get the best ADC accuracy in STM32 microcontrollers* (AN2834).

The figure below shows the basic principle of switched-capacitor SAR ADC principle (for a 10-bit ADC).

Figure 2. Basic schematic of SAR switched-capacitor ADC (10-bit ADC example)



Note: This is a schematic of an ADC with digital output.

In this figure, the input voltage (V_{IN}) is connected through sampling switch (Sa) to the whole capacitive network that works as sampling capacitor (its charging duration defines the sampling time, Sb is closed). The whole capacitive network is charged to V_{IN} voltage. Then the Sa switches from V_{IN} to V_{REF} and Sb is open. Then the successive approximation is performed: in each clock cycle, the switches S1 to S11 are rearranged and the comparator compares the final voltage. During each S1 to S11 switches rearrangement, there is a charge redistribution between capacitors.

2.4 Parasitic components

In each approximation step, the charge redistribution between capacitors is performed. This charge redistribution causes current peaks between capacitors and also from V_{REF} voltage (see Figure 2). Those current peaks are limited by the parasitic components: resistance and inductance between capacitors and V_{REF}/V_{SSA} voltage.

At the end of each approximation cycle (ADC clock frequency), all currents must be close to zero because the voltage must be stable for comparator comparison. The speed to reach this stable state during charge redistribution is given by all RLC components. The dominant capacity fraction is the capacity of the capacitors network, respectively rearranged sampling capacitor into serial-parallel combination during the approximation (given by configuration of S1 to S11 switches).

The R and L components are parasitic:

- R represents the resistance: mainly the resistivity of the S1 to S11 switches(and on chip metal paths).
- L represents the inductance of all conductive paths: mainly the longest conductive path from VREF/VSSA pads to VREF/VSSA pins (bonding wires and on chip metal paths).

In practice there are attenuated voltage and current oscillations in each approximation step. For correct operation, the amplitude of voltage oscillations (on comparator, respectively on the capacitor network) must decrease below 1 LSB.

Frequency of oscillations is given by LC components and attenuation is given by RL components. For rapid attenuation, the inductance must be kept at a low value: exponential decrease of oscillations is given by formula:

$e^{-R/(2L).t}$ (envelope of attenuated oscillations at frequency $(2\pi f)^2 = 1 / (LC)$)

The ADC maximum operating frequency is given by those parasitic RL components.

Note: A large decoupling capacitor must be connected directly between the VREF+ and VSSA pins. This capacitor creates an ideal V_{REF} voltage source (fixed DC voltage without oscillations on this decoupling capacitor).

2.5 Application design to reach ADC maximum conversion speed

2.5.1 Decoupling capacitor and PCB design

As mentioned in the previous section, the VREF+ pin must be correctly decoupled.

An appropriate decoupling capacitor must be connected between VREF+ and VSSA pins with a minimum added inductance. Each 1cm of metal path on PCB adds approximately from 6 to 10 nH of inductance. The decoupling capacitor must be placed as close as possible to VREF+ and VSSA pins without through hole connections that may create a loop increasing the inductance.

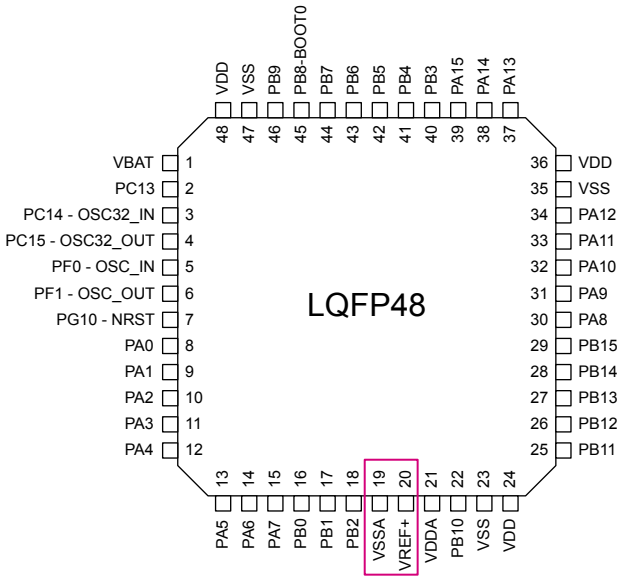
The placement of the decoupling capacitor must be made on the same layer as VREF+ and VSSA pins. The decoupling capacitor must have a low ESR and a low inductance (for example: ceramic capacitor).

2.5.2 Package selection

The internal parasitic inductance depends on the chip layout and also on the distance between the VREF+/VSSA pads on chip and the VREF+/VSSA pins on the package.

This distance is given by the bonding wires and the pins. The pinout of STM32G4 Series MCUs is designed to have a minimum internal inductance: VREF+ and VSSA pins are adjacent, creating then a minimum current loop and minimizing the internal inductance (see the figure below).

Figure 3. Example of VREF+ and VSSA pins location on STM32G4 LQFP48 package



Even though, some packages offer lower distance between chip pads and package pins. For example, the internal inductance is larger on LQFP packages than on UFBGA, UFQFPN or WLCSP packages, due to longer wires from pads to pins.

To decrease even more the inductance on large packages (such as the high-pin count LQFP128) has a VREF+ signal connected by two wires to the two VREF+ pins.

2.5.3 Decrease of ADC clock frequency

If the PCB design is not good enough and if there is an additional external inductance, the oscillations are not attenuated below 1 LSB at the end of the approximation cycle (equal to ADC clock cycle). In this case the ADC may produce DNL errors at high ADC clock frequency.

The solution is to decrease the ADC clock frequency with keeping, if possible, the required final data sampling rate.: slow down each approximation cycle and wait more time for attenuation.

Application example

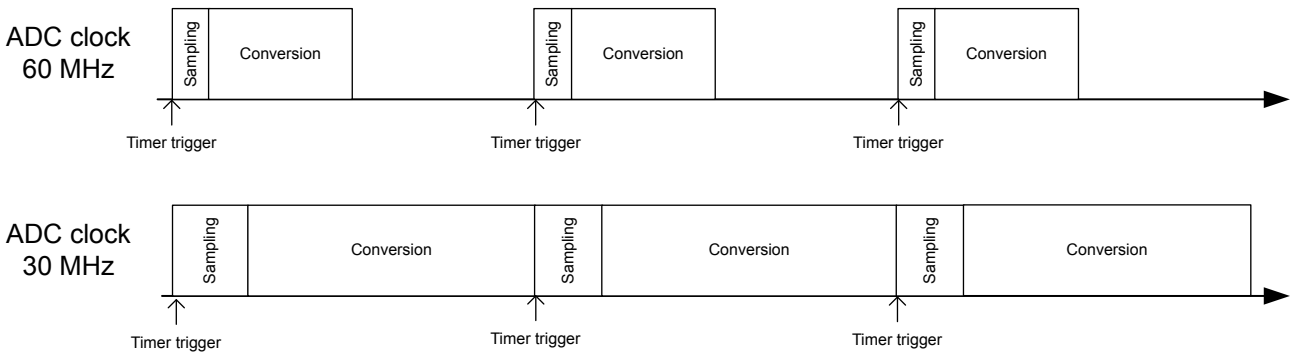
In this example:

- The ADC is triggered by a timer at a 2 MHz trigger frequency (ADC conversion triggered every 500 ns).

- The ADC clock is 60 MHz.
- The sampling time is 2.5 ADC clock cycle.
- The conversion time is 15 ADC clock cycles (250 ns).
- The sampling rate is 1 / 250 ns = 4 Msps.

The ADC frequency can be decreased down to 30 MHz (each approximation cycle is then two times longer), while keeping the timer trigger frequency at 2 MHz.

Figure 4. Example ADC frequency decrease while keeping the final data rate



2.6 STM32G4 multiple ADCs and parallel operations

2.6.1 Parasitic oscillations influences

Up to five ADC instances are implemented in the STM32G4 Series MCUs. More than one ADC is used at one time in the applications, means various ADCs conversions happen at the same time. This ADCs parallel operation may influence the final ADCs results.

The effect of parasitic RLC components to conversion speed is explained in Section 2.4 . In case of parallel ADCs operation, all the ADCs use the same V_{REF} voltage. The schematic diagram in Figure 2 is therefore multiplied but the V_{REF} voltage remains common for all ADCs. There are more capacitors networks connected in parallel to V_{REF}. More capacity change in each approximation step causes higher current peaks from V_{REF} and the internal oscillations have then higher amplitude. The frequency of oscillations decreases due to larger capacity connected to V_{REF}.

Due to all those effects, the attenuation reaches 1 LSB level later and the maximum ADC frequency of all parallel operating ADCs is lower than in case of only one ADC. If the ADCs clock is kept high, the attenuation does not decrease below 1 LSB level and the ADCs produce DNL errors. There is also an interference between the ADCs: one ADC influences another ADC result. This influence depends on the synchronization between the ADCs: when a given ADC starts an approximation regarding to another ADC. The ADC frequency must be decreased to keep the ADCs results accurate (each approximation cycle is extended).

2.6.2 Optimizations for multiple ADCs operation

The suggestions for the design of an application using multiple ADCs operation are the same than for a single ADC (refer to Section 2.5): good VREF+/VSSA pins decoupling, correct VSSA grounding.

For multiple ADCs operation, all the effects of the internal oscillations and charging currents from V_{REF} are cumulated (from all used ADCs). A correct PCB design is therefore very important: take care of the decoupling of VREF+ pin and the correct grounding layout, because there are relatively high current peaks on the VREF+ pin.

Note: The unstable voltage on VREF+ pin can influence the DAC performance because VREF+ pin provides reference voltage for the DAC.

3 ADC limitation: input channel switch disturbs ongoing conversions

3.1 Limitation description

This limitation is described in the errata sheets of the STM32G4 Series MCUs. More details and possible workarounds are detailed below.

Each ADC has an input multiplexer that performs the selection of a given channel: there are sets of analog switches between the ADC input and a given pin on the package. The Sa sampling switch (see Figure 2) is implemented behind the multiplexer. Sa is switched on during sampling time (initiated by the trigger). During the successive approximation, Sa is open to isolate the capacitors network from the analog input. The multiplexer is switched to the next programmed channel in the middle of the successive approximation (in case of scan mode). If the ADC is used in single mode or at the end of the scan sequence, the multiplexer is switched to the internal channel (Channel 31).

The multiplexer switching from the current channel to the following channel generates some noise that may influence the successive approximation currently in progress (especially the bit under evaluation in the successive approximation sequence). This may also impact the DNL error of any ADC currently converting.

The worst case is when various ADCs operates synchronously and their input multiplexers switch to the next channel at the same clock cycle (usually the case as all ADCs are programmed with the same parameters and triggered by the same trigger). In this case, the noise is cumulated and the DNL error of the ADC results is maximal.

3.2 Workaround

This workaround is based on disabling the input multiplexer switch during the successive approximation.

The input multiplexer switch is not performed in the following cases:

- in continuous conversions for the same channel

  Continuous conversions are performed on the same channel and the input multiplexer is kept switched on the given selected channel (except for the final conversion).
- in bulb mode for the same channel

  The input multiplexer is kept switched on the selected channel (and does not switch to internal channel) because the sampling phase starts immediately after finishing conversion from the same selected channel.
- in scan sequence if the next channel number is the same as current channel number

  The multiplexer switches to the following channel in the middle of the conversion, but no switch is performed if the following channel number is the same as current channel .

The above cases can be used as workaround to solve switching problem. In single channel applications (only one channel per ADC is used), the 'bulb mode for the same channel' use-case is appropriate. In multiple channels applications (various channels per ADC are used), the last use-case is better.

In the last use-case, the original channel scan sequence must be modified that each channel is doubled into pairs in the scan sequence. The correct results are taken only from the first sample of the pair. This solution leads to decrease the effective sampling data rate to one half (each second conversion is thrown). This case offers also a solution if various ADCs are operating together in synchronous operation. In asynchronous ADCs operation, the channel switching noise may influence another ADC as the channel switching is not synchronized among ADCs.

3.3 Optimized channels sequence

For some applications, the proposed workarounds are not suitable. For example, a high data rate is required and doubling each channel in scan sequence impacts too much data rate. In this case the scanned channel sequence can be optimized regarding the channel numbers order.

The noise level generated by the multiplexer channel switch depends on the channel numbers used, especially on the change between current channel number and the following channel number. The generated noise level is proportional to the number of bits changed in the channel number (in case of channel change).

Each number (for example Channel 6) has a binary representation (0110 in the example). If there is a change to the next number (for example to Channel 15 with binary representation 1111), the generated noise is proportional to the number of changed bits in this number (2 bits changed from Ch 6 to Ch 15: 0110 to 1111). Those changed

bits represents the Hamming distance. An optimum channels sequence represents a Gray code sequence. In a Gray code sequence, only one bit is changed between each number change.

Example

For numbers 0-15, the Gray code sequence in binary representation is the following: 0000 to 0001 to 0011 to 0010 to 0110 to 0111 to 0101 to 0100 to 1100 to 1101 to 1111 to 1110 to 1010 to 1011 to 1001 to 1000.

The ADC channels numbers must be carefully selected for the scan sequence, to minimize the impact of this ADC limitation.

When no scan mode is used (channel selected by software before each conversion), the channel switching is performed to the internal channel (in the middle of the conversion). The internal channel is Channel 31 in the ADCs of the STM32G4 Series MCUs. In this case, the workaround with bulb mode only is recommended: optimization with Gray code to number 31 is possible only from number 15: 01111à 11111). The workaround with bulb mode completely removes this ADC limitation.

4 Minimize the ADC errors

4.1 General rules

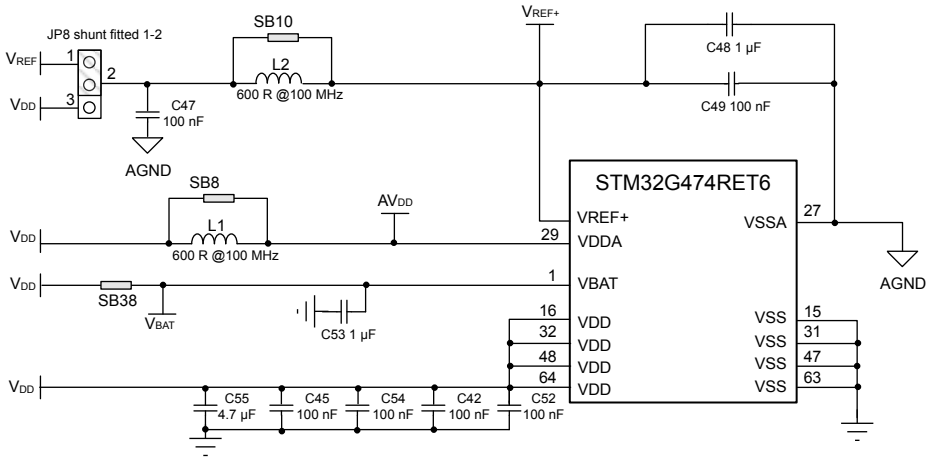
The application note *How to get the best ADC accuracy in STM32 microcontrollers* (AN2834) describes the general rules, methods and recommendations for correct design of applications using ADCs. Refer to this document to design properly any application with STM32G4 Series MCUs ADCs.

4.2 Specific recommendations

The ADCs in STM32G4 Series devices have some specific properties for which the following additional recommendations are defined:

- Reference voltage on VREF+ pin can be also driven from $V_{REFBUFF}$ (internal reference voltage used on VREF+ pin):
  - Use recommended decoupling capacitor on VREF+ pin: 1 µF + 100 nF. Place this capacitor directly between VREF+ and VSSA pins.
  - Take care of the external load connected to VREF+ pin. Driving capability of $V_{REFBUFF}$ is 6.5 mA, that covers also the internal ADCs and DACs consumptions from VREF+ pin. If the application uses more ADCs and DACs, the external driving capability from VREF+ pin decreases proportionally (see the STM32G4 Series datasheets for ADC and DAC current consumptions from VREF+).
- VSSA and VSS grounding:
  - The VSSA pin must be connected as close as possible to the VSS pin. The VSSA pin is used as analog supply (together with VDDA pin) and also as ground reference for V_{REF+} voltage (VSSA pad is internally double bonded with VREF- pad).
  - The PCB design must use a large ground plate for VSS ground and connect VSSA pin directly to this VSS ground plate. If a specific voltage source is used for V_{REF+} (or V_{DDA}), connect this voltage source directly to VREF+/VSSA or VDDA/VSSA pins.
- Filtering of analog supply voltages:
  - Avoid to use of larger inductors as filters for VSSA or VREF+ pins. The inductor together with the decoupling capacitor create an LC filter that operates correctly only if its load is stable (like some resistance on the LC filter output). It filters correctly the input voltage fluctuations. If the LC filter load generates current peaks (like current peaks from VREF+ or VDDA pin), this fast transient current peak can lead to attenuated oscillations of this LC filter at its resonant frequency. In fact, the current peak decreases the voltage on the decoupling capacitor and, because the inductor inhibits large current changes, the capacitor is charged back slowly and the LC circuit may oscillate. These voltage oscillations are present on the decoupling capacitor and therefore, the V_{REF+} or V_{DDA} voltage is influenced. The oscillations on VREF+ or VDDA pin are attenuated after a relative long time (when the current peak disappears) and may influence the V_{REF+} and V_{DDA} voltages in later critical times.
  - In some designs, the high frequency inductor (or better say choke) must be used to filter very high noise from the power supply (if really present). In parallel to this choke footprint, it is recommended to design the solder bridge that can short the choke in case of problems with V_{REF+} or V_{DDA} voltage stability (see the example in the figure below). The ferrite choke must be properly selected to filter very high frequencies (relative to current supply peaks frequency) and their impedance character at high frequencies must be more resistive than inductive (high-frequency losses in the ferrite core).

Figure 5. Example of designing solder bridges (SB8, SB10) in parallel to chokes (L1, L2) on analog supply voltages



- Signal source driving properties knowledge regarding to ADC input properties:
  - The signal source impedance value must be known to correctly design the ADC sampling time. If the signal source has higher impedance, longer sampling times must be used to charge properly the sampling capacitor (see STM32G4 Series devices datasheets for recommended ADC sampling times for various external source impedance). The use of longer sampling time leads to decrease the maximum ADC data rate. For very fast data rate, the use of signal source with low impedance is recommended.
  - To decrease the signal source impedance, an analog buffer can be used as ADC signal source (for example OPAMP in the follower mode). The speed of this analog buffer (slew rate and frequency bandwidth) must be known to correctly program the ADC sampling time. At the beginning of the ADC sampling phase, the discharged sampling capacitor is connected to the analog buffer (OPAMP) output. The voltage on the OPAMP output is zero at this moment (discharged sampling capacitor at OPAMP output). Then the OPAMP (thanks to its feedback) starts compensate this unbalance by increasing the output driving and charging the sampling capacitor. The speed of this OPAMP driving increase depends on the OPAMP speed (propagation of the OPAMP input change to the OPAMP output change). In the example of the OPAMP embedded in STM32G4 Series devices: The OPAMP has a frequency bandwidth of 13 MHz. A first estimation of the propagation delay is 1 / 13 MHz = around 77 ns. The sampling capacitor must then be charged by the OPAMP to 1 LSB accuracy. The recommended ADC sampling time to read the embedded OPAMP output by ADC is 200 ns (see the datasheet). If the ADC clock is for example 60 MHz, the sampling time must be programmed to more than 200 ns x 60 MHz = 12 clock cycles (leading to program sampling time to 12.5 ADC clock cycles, bits SMP[2:0] = 010). The final data rate is then 60 MHz / (12.5 + 12.5) = 2.4 Msps (maximum data rate while using the embedded OPAMP as buffer for ADC).
  - For measurement of signal sources with very high impedance, refer to section 3.4 *High impedance source measurement* of the application note *How to get the best ADC accuracy in STM32 microcontrollers* (AN2834), where some methods for high impedance source measurement and design calculation for practical implementation are detailed.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
14-Jun-2019	1	Initial release.

Contents

List of figures